CLAIMS:

What is claimed is:

1. A radio transmitter within a radio transceiver, comprising:

a digital modulator that receives outgoing digital data, that digitally modulates the outgoing digital data to produce a digital information signal, and that compensates the digital information signal to produce a pre-compensated digital information signal that is pre-compensated for phase and magnitude imbalance of at least one analog downstream radio transceiver circuit component, the digital modulator further including an adder to sum in-phase signal component and quadrature phase signal component of the pre-compensated digital information signal to produce an outgoing signal for transmission;

a digital-to-analog converter (DAC) that receives the pre-compensated digital information signal and that converts the pre-compensated digital information signal to produce a continuous waveform analog signal;

a downstream filter that filters the continuous waveform analog signal to produce a filtered continuous waveform analog signal; and

phase locked loop circuitry (PLL) that receives the filtered continuous waveform analog signal to produce an output information signal in a selected frequency band.

2. The radio transmitter of claim 1 wherein the digital modulator includes a two-part amplification logic wherein a first part of the two-part amplification logic amplifies the in-phase component of the digital information signal by a first amount to produce an in-phase component of the pre-compensated digital information signal that is amplitude compensated and wherein a second of the two-part amplification logic amplifies the in-phase component of the digital information signal by a second amount to produce an in-phase signal component that is summed with the quadrature phase signal component of the digital information signal to produce a

quadrature portion of the pre-compensated digital information signal that is phase and magnitude compensated.

3. The radio transmitter of claim 2 further including compensation logic for producing a compensation control signal to the first part of the two-part amplification logic to individually control amplification levels of the first part of the two-part amplification logic.

4. The radio transmitter of claim 3 wherein the first part of the two-part amplification logic further includes a plurality of selectable amplification modules to provide selectable amounts of constant amplification of the in-phase signal component.

5. The radio transmitter of claim 4 wherein the plurality of selectable amplification modules of the first part of the two-part amplification logic is greater than or equal to five selectable amplification modules and wherein the compensation control signal received by the first part of the two-part amplification logic is at least five bits longfor individually selecting the selectable amplification modules.

6. The radio transmitter of claim 5 further including a selectable inverter for selectably inverting a polarity of a sum of the selectable amounts of constant amplification of the in-phase signal component.

7. The radio transmitter of claim 6 wherein the compensation signal further includes a bit for selecting the inverter.

8. The radio transmitter of claim 2 further including compensation logic for producing a compensation control signal to the second part of the two-part amplification logic to individually control amplification levels of the second part of the two-part amplification logic.

9. The radio transmitter of claim 8 wherein the second part of the two-part amplification logic further includes a plurality of selectable amplification modules to provide selectable amounts of constant amplification of the in-phase signal component.

10. The radio transmitter of claim 9 wherein the plurality of selectable amplification modules of the second part of the two-part amplification logic is greater than or equal to five selectable amplification modules and wherein the compensation signal received by the second part of the two-part amplification logic is at least five bits long for individually selecting the selectable amplification modules.

11. The radio transmitter of claim 10 further including a selectable inverter for selectably inverting a polarity of a sum of the selectable amounts of constant amplification of the in-phase signal component.

12. The radio transmitter of claim 11 wherein the compensation signal further includes a bit for selecting the inverter.

13. The radio transmitter of claim 1 wherein a quadrature phase (Q) portion of the pre-compensated digital information signal includes an in-phase (I) component compensation.

14. The radio transmitter of claim 13 further comprising compensation logic for setting an amount of the in-phase component compensation that is produced to the adder for summing with the quadrature phase portion.

15. The radio transmitter of claim 14 wherein the in-phase component compensation includes an amplified component of a specified amount.

16. The radio transmitter of claim 15 further comprising compensation logic for setting an amount of in-phase component amplification of the in-phase component compensation.

17. A radio receiver, comprising:

a low noise amplifier for receiving an RF signal and for amplifying the RF signal;

phase locked loop circuitry (PLL) that receives the amplified RF signal to produce a down converted in-going continuous waveform signal having in-phase and quadrature phase components;

filtering circuitry that filters the in-going continuous waveform signal to produce filtered continuous waveform in-phase and quadrature phase components;

analog-to-digital converter (ADC) circuitry that receives the filtered continuous waveform in-phase and quadrature phase component and that produces in-going in-phase and quadrature phase digital signals; and

a digital de-modulator that receives in-going in-phase and quadrature phase digital signals, that digitally de-modulates the in-going digital signals to produce digital bits out, and that compensates the in-going in-phase digital signal to produce a compensated digital information signal that is compensated for phase and magnitude imbalance of at least one analog upstream receiver circuit component, the digital de-modulator further including an adder to sum the in-going in-phase digital signal and the in-going quadrature phase digital signal of the in-going in-phase and quadrature phase components of the compensated digital information signal to produce digital bits for processing by a processor.

18. The radio receiver of claim 17 wherein the digital de-modulator includes a two-part amplification logic wherein a first part of the two-part amplification logic amplifies the in-going in-phase digital signal by a first amount to produce an in-phase component of the compensated digital information signal that is amplitude compensated and wherein a second PART of the two-part amplification logic amplifies the quadrature phase digital signal by a second amount to produce a quadrature phase component that is summed with the in-phase component to produce the compensated digital information signal that is phase and magnitude compensated for in-phase and quadrature phase imbalances introduced by upstream analog components.

19. A method for producing an integrated circuit radio transceiver, comprising:

producing an integrated circuit radio transceiver chip;

testing the integrated circuit radio transceiver chip to determine a transceiver operational metric comprising at least one of a transmitter image rejection ratio and a receiver error rate;

evaluating the determined transceiver operational metric to determine whether a specified metric requirement is satisfied;

based upon the evaluating step, determining whether to introduce imbalance compensation in at least one of a receive path or a transmit path;

amplifying an in-phase component in at least one of the receive path and the transmit path;

determining an imbalance compensation amount;

introducing imbalance compensation comprising at least one of amplifying the in-phase component and adding the amplified in-phase component to a quadrature component in the transmit path or amplifying the quadrature phase component and adding the amplified quadrature phase component to the in-phase component in the receive path; and

producing additional integrated circuit radio transceiver chips including the introduced imbalance compensation.

20. The method of claim 19 wherein determining an imbalance compensation amount comprises:

setting an in-phase amplitude amplification constant to unity;

setting a phase amplification constant to zero;

transmitting a test tone;

measuring the transceiver operational metric;

adjusting one of the in-phase amplification constant or phase amplification constant by a first step size and measuring the transceiver operational metric;

adjusting the amplification constant of the previous step by a second step size wherein the second step size is substantially greater than the first step size;

repeating the adjustment steps M times wherein M is equal to a number of selectable amplification adjustments to one of the in-phase amplitude amplification constant or the phase amplification constant.

21. The method of claim 20 wherein the method is terminated once one of the transmitter image rejection ratio or the receiver error rate metric satisfy respective specified values.

22. The method of claim 21 wherein the method is terminated after no more than (4 * M + 1) iterations.